Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **VCC**

**.047”**

**54**

**LSR**

**86**

**B**

**MASK**

**REF**

**6 7 8 9**

**2 1 14 13 12**

**11**

**10**

**3**

**4**

**5**

**.045”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .045” X .047” DATE: 5/18/21**

**MFG: NATIONAL-FCH THICKNESS .012” P/N: 54LSR86**

**DG 10.1.2**

#### Rev B, 7/19/02